SYSTEMS AND METHODS FOR FORMING MULTIPLE FIN STRUCTURES USING METAL-INDUCED-CRYSTALLIZATION

FIELD OF THE INVENTION

[0001] The present invention relates generally to semiconductor manufacturing and, more particularly, to FinFET devices that include multiple silicon fin structures and a method for forming the fin structures.

BACKGROUND OF THE INVENTION

[0002] Scaling of device dimensions has been a primary factor driving improvements in integrated circuit performance and reduction in integrated circuit cost. Due to limitations associated with gate-oxide thicknesses and source/drain (S/D) junction depths, scaling of existing bulk MOSFET devices below the 0.1 μm process generation may be difficult, if not impossible. New device structures and new materials, thus, are likely to be needed to improve FET performance.

[0003] Double-gate MOSFETs represent devices that are candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, the use of two gates to control the channel significantly suppresses short-channel effects. A FinFET is a double-gate structure that includes a channel formed in a vertical fin. Although a double-gate structure, the FinFET is similar to existing planar MOSFETs in layout and fabrication techniques. The FinFET also provides a range of channel lengths, CMOS compatibility, and large packing density compared to other double-gate structures.

SUMMARY OF THE INVENTION

[0004] Implementations consistent with the principles of the invention provide multiple silicon fin structures formed on a semiconductor device. The multiple fin structures may, in implementations consistent with the principles of the invention, have a very small pitch.

[0005] In accordance with the purpose of this invention as embodied and broadly described herein, a method facilitates the forming of fin structures for a semiconductor device that includes a substrate and a dielectric layer formed on the substrate. The method includes etching the dielectric layer to form a first structure, depositing an amorphous silicon layer over the first structure, and etching the amorphous silicon layer to form second and third fin structures adjacent first and second side surfaces of the first structure. The second and third fin structures may include amorphous silicon material. The method further includes depositing a metal layer on upper surfaces of the second and third fin structures, performing a metal-induced crystallization operation to convert the amorphous silicon material of the second and third fin structures to a crystalline silicon material, and removing the first structure.

[0006] According to another aspect of the invention, a semiconductor device is provided. The semiconductor device includes multiple fin structures that include a crystalline silicon material. The semiconductor device further includes a source region formed at one end of the fin structures, a drain region formed at an opposite end of the fin structures, and at least one gate.

[0007] According to yet another aspect of the invention, a semiconductor device is provided. The semiconductor device includes a substrate, multiple crystalline silicon fin structures formed on the substrate, a source region formed at one end of the fin structures, a drain region formed at an opposite end of the fin structures, and one or more gates. A center-to-center distance between each of the fin structures is about 600 Å.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, explain the invention. In the drawings,

[0009] Fig. 1 illustrates an exemplary process for forming fin structures for a FinFET device in an implementation consistent with the principles of the invention;

[0010] Figs. 2-8 illustrate exemplary views of a FinFET device fabricated according to the processing described in Fig. 1;

[0011] Fig. 9 is an exemplary graph illustrating negative resistance behavior; and

[0012] Fig. 10 is a diagram of exemplary triangular spacers.

DETAILED DESCRIPTION

[0013] The following detailed description of implementations consistent with the present invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

[0014] Implementations consistent with the principles of the invention provide crystalline silicon fin structures that are formed on a semiconductor device. FinFET channel width is defined by the height of the fin. The fin height is typically limited due to patterning concerns, affecting the drive current. Implementations consistent with the principles of the invention use multiple fin structures in order to achieve the desired drive current. For area efficiency, the multiple fin structures may be densely provided (i.e., formed in close proximity to each other).

EXEMPLARY PROCESSING

[0015] Fig. 1 illustrates an exemplary process for forming fin structures for a FinFET device in accordance with an implementation consistent with the principles of the invention. Figs. 2-8 illustrate exemplary views of a FinFET device fabricated according to the processing described with respect to Fig. 1. The fabrication of one FinFET device will be described hereinafter. It will be appreciated, however, that the techniques described herein are equally applicable to forming more than one FinFET device.

[0016] With reference to Figs. 1 and 2, processing may begin by forming a dielectric structure 210 on a substrate 200 of a semiconductor device (act 110). In one implementation, substrate 200 may include silicon. In alternative implementations consistent with the present invention, substrate 200 may include other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. In another alternative, substrate 200 may include an insulator, such as an oxide layer, formed on a silicon or germanium layer. Dielectric structure 210 may include a dielectric material, such as an oxide or a nitride.

[0017] Dielectric structure 210 may be formed in a conventional manner. For example, a dielectric material, such as an oxide material (e.g., SiO_2) may be deposited over substrate 200 to a thickness ranging from about 500 Å to about 2000 Å. A mask may be formed over a portion of the dielectric material and the dielectric material may then be etched in a conventional manner, with the etching terminating on substrate 200 to form dielectric structure 210. Further thinning of dielectric structure 210 may be achieved by an additional conventional etching process. The resulting dielectric structure 210 may have a width ranging from about 200 Å to about 1000 Å.

[0018] After forming dielectric structure 210, an amorphous silicon layer 310 may be deposited on the semiconductor device, as illustrated in Fig. 3 (act 120). In one implementation

consistent with the principles of the invention, amorphous silicon layer 310 may be deposited to a thickness ranging from about 100 Å to about 1000 Å.

[0019] Amorphous silicon layer 310 may then be etched in a conventional manner, with the etching terminating at substrate 200 to form amorphous silicon fin structures 410, as illustrated in Fig. 4 (act 130). Each amorphous silicon fin structure 410 may have a height ranging from about 500 Å to about 2000 Å and a width ranging from about 100 Å to about 1000 Å.

[0020] A thin metal layer 510, such as nickel, may be deposited on the semiconductor device, as illustrated in Fig. 5 (act 140). For example, a mask may be used to facilitate the deposition of nickel layer 510 over amorphous silicon fin structures 410, as illustrated in Fig. 5. In one implementation, nickel layer 510 may be deposited to a thickness of about 20 Å.

[0021] A metal-induced-crystallization (MIC) operation may then be performed. The MIC operation may involve annealing nickel layer 510 at about 500 °C to about 550 °C for several hours, which acts to diffuse the nickel into the amorphous silicon to convert the amorphous silicon in fin structures 410 to crystalline silicon fin structures 610, as illustrated in Fig. 6 (act 150).

[0022] After crystalline silicon fin structures 610 are formed, dielectric structure 210 may be removed, as illustrated in Fig. 7 (act 160). For example, a conventional etching technique selective to the material in dielectric structure 210 may be used to remove dielectric structure 210, while minimizing effects to crystalline silicon fin structures 610. Alternatively, a mask may be formed over fin structures 610 to protect fin structures 610 during the etching. The etching of dielectric structure 210 may terminate on substrate 200, as illustrated in Fig. 7.

[0023] The resulting fin structures 610, consistent with the present invention, may have a small pitch (i.e., center-to-center distance between fin structures 610). For example, the pitch for fin structures 610 may be as small as about 300 Å.

[0024] Once dielectric structure 210 is removed, conventional FinFET fabrication processing can be used to complete the transistor (e.g., forming the source and drain regions, contacts, interconnects and inter-level dielectrics for the FinFET device). For example, a protective dielectric layer, such as a silicon nitride or silicon oxide may be formed on the top surface of fin structures 610, followed by the formation of a gate dielectric on the side surfaces of fin structures 610. Source/drain regions may then be formed at the respective ends of fin structures 610, followed by formation of one or more gates. For example, a silicon layer, germanium layer, combinations of silicon and germanium or various metals may be used as the gate material. The gate material may then be patterned and etched to form the gate electrodes.

[0025] For example, Fig. 8 illustrates an exemplary top view of the semiconductor device consistent with the principles of the invention after the source/drain regions and gate electrodes are formed. As illustrated, the semiconductor device includes a double-gate structure with fin structures 610, source and drain regions 810 and 820, and gate electrodes 830 and 840.

[0026] Source/drain regions 810 and 820 may then be doped with n-type or p-type impurities based on the particular end device requirements. In addition, sidewall spacers may optionally be formed prior to the source/drain ion implantation to control the location of the source/drain junctions based on the particular circuit requirements. Activation annealing may then be performed to activate source/drain regions 810 and 820.

[0027] A FinFET device, as described above, is formed with two crystalline silicon fin structures. It should be understood that methods consistent with the present invention may be

used to form any number of fin structures, such as more than two fin structures, based on the particular circuit requirements. In this case, additional dielectric structures may also be formed.

OTHER IMPLEMENTATIONS

[0028] Heavily doped channel FinFETs exhibit behavior similar to that exhibited by negative resistance devices. The negative resistance device behavior may be used to form a static random access memory (SRAM). Fig. 9 is an exemplary graph illustrating this negative resistance behavior.

[0029] It is sometimes desirable to create a triangular spacer for a FinFET device because it facilitates polysilicon patterning for the FinFET device. Fig. 10 is a diagram of exemplary triangular spacers. For example, a polysilicon layer 1010 may be deposited over a semiconductor device. Polysilicon layer 1010 may then be etched to form triangular spacers 1020. Certain deposition and etching techniques are known to those skilled in the art to create smooth triangular spacers 1020, as illustrated in Fig. 10, as opposed to step spacers (e.g., the spacers created as shown in Figs. 3 and 4).

CONCLUSION

[0030] Implementations consistent with the principles of the invention provide multiple crystalline silicon fin structures for a FinFET device. The multiple fin structures may be densely provided so as to have a very small pitch.

[0031] The foregoing description of exemplary embodiments of the present invention provides illustration and description, but is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention.

[0032] For example, in the above descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough

understanding of the present invention. However, the present invention can be practiced without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional deposition, photolithographic and etching techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

[0033] While a series of acts has been described with regard to Fig. 1, the order of the acts may be varied in other implementations consistent with the present invention. Moreover, non-dependent acts may be implemented in parallel.

[0034] No element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where only one item is intended, the term "one" or similar language is used. The scope of the invention is defined by the claims and their equivalents.